

REMARKS

The Examiner is thanked for the performance of a thorough search. In response to the Office Action mailed February 15, 2002, claims 21, 22, and 23 have been added, claims 1, 8 and 18 have been amended, and claims 2 and 9 have been canceled. All issues raised in the Office Action are addressed herein. No new matter has been added. Claims 1, 3-8, and 10-23 are currently pending in this Application. Applicants respectfully request the reconsideration of the application.

Rejections Under 35 U.S.C. 103(a)

Claims 1-4, 6, 8-11, 13, and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryum et al., hereinafter Ryum (US Patent No. 6,337,494) in view of Kubota (US Patent No. 6,323,530).

Claims 5, 7, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryum in view of Kubota, as applied in claim 1 above, and further in view of Streetman (Solid State Electronic Devices).

Cited Art

Ryum discloses a super self-aligned heterojunction bipolar transistor which is capable of miniaturizing an element, simplifying the process step thereof without using a trench isolation process and sophisticated epitaxial growth processes.

Kubota discloses an optical diode device including a dummy mesa stripe formed on the semiconductor substrate, having a wider top surface as compared to the conventional optical semiconductor, allowing for an upper electrode with relatively wide area and an improved connection between the device and the mount base in a face-down mounting.

combination of Ryum with Kubota would not produce the bipolar transistor of the present invention.

Claims 3-7, 10-17, and 19-20 directly or indirectly depend from and contain all the patentably distinguishing limitations of allowable independent claims 1, 8 and 18 respectively. Therefore, Applicants respectfully submit that dependent claims 3-7, 10-17, and 19-20 are patentable for at least the same reasons as the independent claims from which they depend, and respectfully request the Examiner to withdraw the rejection.

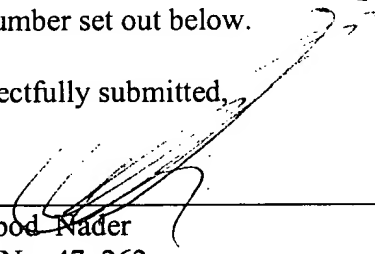
Ciaims 2, and 9 were canceled and the claimed elements were incorporated into claims 1, 8 and 18.

Conclusion

For the forgoing reasons, Applicants submit that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,

DATE: April 25, 2002



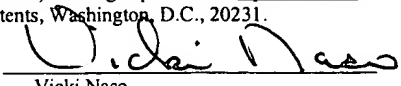
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CERTIFICATE OF MAILING (37 CFR 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited on April 25, 2002, with the U.S. Postal Service as first class mail in an envelope addressed to: Commissioner of Patents, Washington, D.C., 20231.

Date: April 25, 2002



Vicki Naso

Marked up version of the claims

In the claims

Please amend the claims as follows:

1. (Amended) A method for forming a super self-aligned bipolar transistor, comprising the steps of:

providing a semiconductor substrate having a buried collector region;

providing multiple layers above said collector region;

providing an emitter window mask above said multiple layers;

providing three vertical etchings of said multiple layers;

providing a doping of said collector region wherein the doped collector region is determined by the emitter window mask;

providing a horizontal etching of one of said multiple layers, wherein the step of providing a horizontal etching determines that the dimensions of the base region are wider than the dimensions of the doped collector region and the emitter region;

providing a wet etching to remove a final one of said multiple layers; and

providing a base region above said collector region in the horizontally etched area;

providing an emitter region above the base region so that the emitter, base and collector regions are super self-aligned.

8. (Amended) A super self-aligned bipolar transistor apparatus, comprising:

a semiconductor substrate having a buried collector region;

multiple layers above said collector region;

an emitter window mask above said multiple layers;

a doped collector region wherein the width of the doped collector region are equal to the emitter window mask width;

a horizontally etched region of one of said multiple layers, wherein the dimensions of the horizontally etched region determine that the dimensions of the base region are wider than the doped collector region and the emitter region of the transistor;

a base region above said collector region in the horizontally etched region;

an emitter region above the base region so that the emitter, base and collector regions are super self-aligned.

18. (Amended) A method for forming a super self-aligned bipolar transistor, comprising the steps of:

providing a silicon semiconductor substrate having a buried collector region;

providing a first oxide layer, a polysilicon layer, and a second oxide layer above said collector region;

providing a Nitride emitter window mask above said oxide and polysilicon layers;

providing a wet etching with hydrofluoric acid solutions to etch said first and second oxide layers;

providing a horizontal plasma etching of said polysilicon layer, wherein the dimensions of the horizontally etched region determine that the dimensions of the base region are wider than the doped collector region and the emitter region of the transistor;

providing a doping of said collector region wherein the doped collector region is determined by the emitter window mask;

providing a base region above said collector region in the horizontally etched area; wherein the base region extends horizontally beyond the doped collector region;

providing an emitter region above the base region so that the emitter, base and collector regions are super self-aligned.

21. (New) A method for forming a super self-aligned bipolar transistor, comprising the steps of:

providing a semiconductor substrate having a buried collector region;

providing multiple layers above said collector region;
providing an emitter window mask above said multiple layers;
providing three vertical etchings of said multiple layers;
providing a doping of said collector region wherein the doped collector region is determined by the emitter window mask;
providing a horizontal etching of one of said multiple layers, wherein the step of providing a horizontal etching determines that the dimensions of the base region are wider than the dimensions of the doped collector region and the emitter region;
providing a wet etching to remove a final one of said multiple layers; and
providing a base region above said collector region in the horizontally etched area;
providing an emitter region above the base region so that the emitter, base and collector regions are super self-aligned.

22. (New) The method of claim 21 wherein the horizontal etching is performed to a distance greater than the polysilicon layer thickness, and whereby the distance may be conformed to provide desired electrical characteristics.

23. (New) The method of claim 22 wherein the desired electrical characteristics are transistor gain and frequency response.